Request Request Request Request Request

PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	OCuLink Memory Map Correction ECR
DATE:	December 6, 2018
AFFECTED DOCUMENT:	OCuLink Memory Map ECN
SPONSOR:	Jason Stuhlsatz (Broadcom), Alex Haser (Molex)

Part I

1. Summary of the Functional Changes

This is a modification of the cable assembly memory map defined in the OCuLink Memory Map ECN. Some bits contained within the external cable assembly's memory are modified to allow for cable aggregation.

2. Benefits as a Result of the Changes

This aligns the OCuLink specification with the External Cable Specification for a common firmware development effort of cabled PCIe interfaces. The External Cable Specification 3.0 is aligned with the SFF-8636 specification that defines these memory maps and cannot be changed to match the released OCuLink specification.

The OCuLink specification was locked before the External Cable Specification was aligned with the SFF working group.

3. Assessment of the Impact

Existing external OCuLink cable assemblies and ports must be modified to accept the new memory map organization.

4. Analysis of the Hardware Implications

The data contained in the memory within the external OCuLink cable assembly is changed from the current ECN.

5. Analysis of the Software Implications

System management firmware should be modified to check the Identifier field in order to determine which memory map structure is implemented by the cable assembly. System management firmware must be updated to support the new memory map structure.

6. Analysis of the C&I Test Implications

None, C&I does not currently exist.

Request Request Request Request Request

Part II

Detailed Description of the change

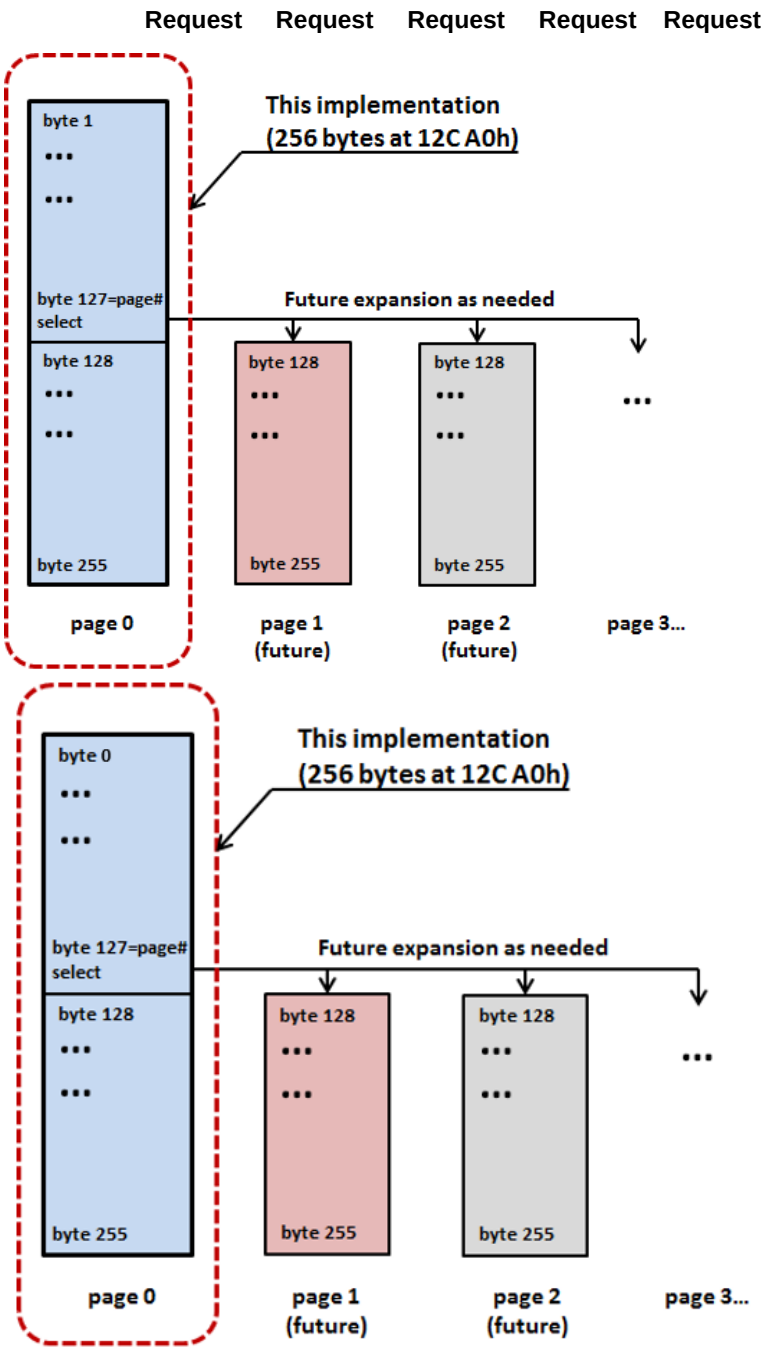
Change Sections A, A.1 and A.2 as follows:

Appendix A – Cable Management Memory Map

This appendix defines the memory map for the cable management interface. The structure of the map is shown in Figure A-1~~Figure A-1~~.

The map is arranged into a single lower page address space of 128 bytes and one mandatory upper address page. Additional upper address pages are not defined in this Specification, but may be used in future expansions.

Formatted: Font: 10 pt, Not Bold


Request
Request
Request
Request
Request
This implementation
(256 bytes at 12C A0h)
byte 1
byte 127=page# select
byte 128
byte 255
Future expansion as needed
byte 128
byte 255
byte 128
byte 255
page 0
page 1 (future)
page 2 (future)
page 3...
This implementation
(256 bytes at 12C A0h)
byte 0
byte 127=page# select
byte 128
byte 255
Future expansion as needed
byte 128
byte 255
byte 128
byte 255
page 0
page 1 (future)
page 2 (future)
page 3...

Request Request Request Request Request

Figure A-1. Cable Management Interface Memory Map

Unless specifically noted, all informative ID fields must contain accurate data. Unless specifically noted, using a value of zero to indicate a field is unspecified is not permitted. Reserved memory locations, labeled Rsvd, are to be filled with logical zeroes in all bit locations for reserved bytes, and in reserved bit locations for partially specified byte locations as described in this appendix. The values are reserved for future use by the PCISIG.

A.1. Lower Page Memory Map

The lower 128 bytes of page 00h are used to access a variety of cable information data. In addition, a mechanism to select upper memory map pages is provided. This portion of the address space is always directly addressable and, thus, is chosen for monitoring and control functions, which may need to be repeatedly accessed.

Request Request Request Request Request

Table A-1. Bytes 0 to 127 (Lower Memory Fields)

Byte	Description	Value	Type	Notes
0	Identifier	0Eh18Ch	Read Only	New Identifier for PCIe Express OCuLink x4. In the 1.0 specification, this field contained 0Eh. If this value is read by firmware, then the memory map structure from the 1.0 specification must be used.
1- to 2	Status – Flat or paged		Read Only	See Table A-2Table A-2
3 122 to 107	RsvdpP			
108 to 109	Propagation Delay		Read Only	One-way propagation delay in nanoseconds (see Section A.1.2x)
110	RsvdP			
111	PCIe Capabilities 1 (see Table A-x)		Read Only	
112	PCIe Capabilities 2 (see Table A-y)		Read Only	
113 to 118	RsvdP			
119 to 122	Password Change (optional)		Write-Only or RsvdP	See Section A.1.3
123 to 126	Password eEntry (optional)		Read/Write-Only or Rsvd	Factory access See Section A.1.3
124	Password entry		Read/Write	Factory access
125	Password entry		Read/Write	Factory access
126	Password entry		Read/Write	Factory access
127	Page Select Byte		Read Only/Write	For future expansion (see Section A.1.4)

Formatted Table

Formatted: Font: 10 pt, Not Bold

A.1.1. Identifier

Insert the same identifier value 0Eh18h into Byte 0 in the lower page (see Table A-1Table A-1) and Byte 128 in the upper page 00h (see Table A- 3, Byte 128).

Formatted: Font: 10 pt, Not Bold

A.1.2. Status

The Status indicator is used to indicate whether flat or paged memory is implemented and is defined in Table A-2Table A-2.

Formatted: Font: 10 pt, Not Bold

Request Request Request Request Request

Table A-2. Status Indicators

Address	Bit	Name	Description
1	7:0All	Rsvdz	
2 2	7:3	Rsvdz	
	02	Flat_mem	Upper memory flat or paged. Flat memory: 0 = paging, 1 = page 00h only
	1:01 7	Rsvdz	

Editor's note: Insert before A.1.3.

A.1.2x. Propagation Delay

This is a 16 bit field to provide the one-way propagation delay through the cable assembly, pin-to-pin, in nanoseconds with fractional values rounded up. Byte 108 bit 7 is the most significant bit and Byte 109 bit 0 is the least significant bit. This information can be useful to the system to derive latency and timing information.

A.1.2y. Cabled PCIe Capabilities 1

The Cabled PCIe Capabilities 1 register specifies capabilities supported by the cable assembly. The bit definitions and values are specified in Table A.x.

Table A-x. PCIe Capabilities 1 Bits (Address 111)

Bit	Description
7:3	Rsvdp
2	1b Set if 8.0 GT/s capable, else Cleared0b
1	1b Set if 5.0 GT/s capable, else Cleared0b
0	Must be Set indicating 2.5 GT/s, capablemust be set to 1b

Editor's note: Adjust formatting so the following text so it appears like the note on page 24 of the OCuLink 1.0 Specification.

Note: While the External Cabling Sspecification defines bits 5 and 7,6 it isthey are not applicable to this specification and areis defined here as reserved and areis labeled Rsvdp.

A.1.2z. Cabled PCIe Capabilities 2

The Cabled PCIe Capabilities 2 register specifies capabilities supported by the cable assembly. The bit definitions and values are specified in Table A-y.

Request Request Request Request Request

Table A-y. PCIe Capabilities 2 Bits (Address 112)

Bit	Description
7	Support for sideband messages
~~7~~6:~~3~~5	Rsvd~~P~~
4:3	Subcable ID 00b – lanes 0-3 01b – lanes 4-7 10b – lanes 8-11 11b – lanes 12-15
2:0	Cable Assembly Logical Width
	000b – x1
	001b – x2
	010b – x4
	011b – x8
	100b – x12
	101b – x16
	All other values are Reserved

A.1.~~3~~6. Password Change and Password Entry

Bytes 119~~123~~ to 126 are ~~reserved~~used for ~~an~~ the optional password entry function. If this function is not supported, all these bytes are Rsvd~~P~~. Byte 123 bit 7 is the most significant bit and Byte 126 bit 0 is the least significant bit. Similary, Byte 119 bit 7 is the most significant bit and Byte 122 bit 0 is the least significant bit.

Password entry field is ~~bytes are~~ retained until power down, reset, or rewritten by the ~~Host System~~Fixed-side. The Password Change field is discarded once the written value has updated the password. These fields are write-only.

~~Additionally, c~~Cable vendors are permitted to use this function to implement write protection of ~~Serial ID~~upper page 00h and other read only information. Password access must not be required to access Free-side device data in either the lower memory page 00h or upper page 00h. Note that multiple manufacturer passwords are permitted to be defined to allow selective access to read or write to various sections of memory, as allowed above.

~~Host system~~ Fixed-side sub-system manufacturer and cable manufacturer passwords must be distinguished by the high order bit (bit 7, byte 123). All ~~Host system~~Fixed-side sub-system manufacturer passwords must fall in the range of 0000 0000h to 7FFF FFFFh, and all cable manufacturer passwords in the range of 8000 0000h to FFFF FFFFh. ~~System~~ Fixed-side sub-system manufacturer passwords must be initially set to 0000 1011h in new cables.

Passwords are permitted to be changed by writing a new password in Bytes 119 to 122 while the correct current password has been entered in 123 to 126, with the high order bit being ignored and forced to a

Request Request Request Request Request

value of 0b in the new password. When the Password Change field is written, the new password value must immediately come into effect, blocking all password protected information, until the Password Entry field contains the new password value.

The current password value(s) must be retained through power cycling or reset. It is strongly recommended that cable assembly vendors provide some vendor-specific method to return the password value(s) to its original factory value.

The Password Entry field shall be set to 0000 0000h on power up and reset.

A.1.~~47~~. Page Select

Byte 127 is used to select the upper page. A value of 00h indicates upper memory page 00h is available to be mapped to locations 128 to 255. All other values are Reserved for future use.

A.2. Upper Page Memory Map

The upper page 00h contains the serial identifiers and is used for read-only identification information. The serial identifier is divided into the base ~~level~~ identifier fields (bytes 128 to 191), extended identifier fields (bytes 192 to 223), and vendor-specific data fields (bytes 224 to 255). The format of the ~~Serial ID~~upper page 00h Memory Map is shown in Table A-3.

Table A-3. Upper Page 00h

Byte	Description	Value	Type	Notes
128	Identifier	~~0Eh~~18~~Ch~~	Read Only	~~New PCIe Identifier~~See Notes for Byte 0 located in Table A-1~~Table A-1~~
129	Extended Identifier		Read Only	See Table A-4
130	Rsvd~~P~~			
131	Peripheral Power ~~5~~Supported	Bit 0: ~~two Lanes~~5 V supported 0 = no 1 = yes Bits 7:-1 - Rsvd~~P~~	Read Only	
132~~-138~~ to 146	Rsvd~~P~~			
~~139~~	~~Number of Lanes~~	~~Bits 2:0~~ ~~001b = 1 Lane~~ ~~010b = 2 Lanes~~ ~~100b = 4 Lanes~~ ~~All others RsvdP~~ ~~Bits 7:3 RsydP~~	~~Read Only~~	~~Value 3 is not a valid entry for this field~~
~~140~~	~~Supported PCIe rates~~	~~Data Rate Identifier~~ ~~Bit 0 RsvdP~~	~~Read Only~~	~~Nominal PCIe Bit Rate; this enables support for Legacy Cables and for future upgrades~~

Formatted: Font: 10 pt, Not Bold

Request Request Request Request Request

Byte	Description	Value	Type	Notes
		Bit 1 – 2.5 GT/s Data Rate Bit 2 – 5.0 GT/s Data Rate Bit 3 – 8.0 GT/s Data Rate Bits 7:4 – RsvdP.		
141 - 142	RsvdP			
143 – 144	Propagation delay	16-bit hex number	Read Only	
145 - 146	RsvdP			
147	Cable Technology		Read Only	See Table A-5 and A-6
148 - to 163	Vendor Name	ASCII string (16 char)	Read Only	See Section A.4
164	RsvdP			
165 - to 166	PCI-SIG Vendor ID	Hex number 2 bytes	Read Only	See Section A.4.1
167	RsvdP			
168 - to 183	Vendor Part Number	ASCII string (16 char)	Read Only	See Section A.4.2
184 - to 185	Vendor Revision	Hex number (2 bytes)ASCII string (2 char)	Read Only	See Section A.4.3
186 - to 189	Copper Cable Attenuation	Hex number	Read Only	Copper cable attenuation, in units of 1 dB, at: 1.25 GHz (Adr 186), 2.5 GHz (Adr 187), 4.0 GHz (Adr 188), and 8.0 GHz (Adr 189); values of all zeroes must be used for an active cable. See Section A.4.4.
190	Max. cCase tTemp	Hex Number	Read Only	Maximum case temperature of cable assembly in degrees Celsius. Is permitted to be all zeroes reporting (if unspecified, 70 °C is assumed).
191	Checksum Base	Low order 8 bits of the sum of the contents of bytes 128 - to 190, discarding any carry out	Read Only	Checksum of Base ID fields bytes (128 - to 190)
192 - to 195	RsvdP			
196 - to 211	Vendor Serial Number	ASCII string (16 Char)	Read Only	Serial number provided by vendor (is permitted to be blank).

Request Request Request Request Request

Byte	Description	Value	Type	Notes
				See Section A.4.5.
212- to 217	Vendor Date Code	ASCII string (yymmdd)	Read Only	Vendor date code (is permitted to be blank)
218- to 219	Vendor Lot Code	Hex number (2 bytes)	Read Only	Vendor lot code (is permitted to be blank)
220- to 222	Rsvd~~P~~			
223	Checksum Extended	Low order 8 bits of the sum of the contents of bytes 192- to 222, discarding any carry out	Read Only	Checksum of Extended ID fields (bytes 192- to 222)
224- to 255	Vendor Specific Data	The format of this data is vendor-specific	Read Only	Vendor-specific data

A.4.4. Copper Cable Attenuation

When the cable is identified as passive copper cable (see Table A-3, Byte 147), these bytes ~~will be~~are used to ~~define~~ report the cable attenuation. A value of all zeroes indicates that the attenuation is not known or is unavailable.